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Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs: Survey Paper

Yashaswini M A, Suchi C, Sinchana V Bhat, Tanuja C

Department of Electronics and Communication Engineering,
Dayananda Sagar Academy of Technology and Management, Bangalore, Karnataka, India

ABSTRACT

This paper presents a detailed review and analysis of key advancements in modeling and understanding short-channel effects in advanced MOSFET architectures, including double-gate and carbon nanotube FETs. Emphasis is placed on electrostatic scale lengths, quantum transport, phonon scattering, and circuit-level implications of nanoscale device behavior. The study compiles and critiques influential models and simulations that guide the design of high-performance, low-leakage transistors compatible with future CMOS technologies.

KEYWORDS: *Short channel effect, quantum transport, Photon scattering, Nanotube FETs, low leakage transistors, double gate*

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INTRODUCTION

The paper "Generalized Scale Length for Two-Dimensional Effects in MOSFET's" by David J. Frank, Yuan Taur, and Hon-Sum P. Wong presents a rigorous analytical derivation of a generalized scale length to better account for two-dimensional (2-D) electrostatic effects in modern MOSFET devices. As device dimensions continue to scale down, traditional one - dimensional models fall short in capturing critical phenomena like drain-induced barrier lowering (DIBL) and threshold voltage rolloff. The authors address this by incorporating the dielectric constant mismatch between the silicon channel and the gate insulator into a new scale length expression. Their formulation is particularly important for evaluating the effectiveness of high-permittivity (high-κ) dielectrics and offers insights into optimal insulator thicknesses for advanced device scaling, including implications for double-gate FET architectures.[1]

In their influential work, Frank et al. (1998) addressed a critical limitation in conventional MOSFET scaling theory by introducing a generalized scale length formulation to account for two-dimensional (2-D) electrostatic effects in short-channel devices. Traditional one-dimensional models often neglect the dielectric mismatch between the silicon substrate and high-permittivity gate insulators, leading to inaccurate predictions of short-channel behavior such as drain-induced barrier lowering (DIBL) and threshold voltage rolloff. By incorporating the permittivity contrast and solving the potential distribution analytically, this paper provides a more precise estimation of scale length and highlights constraints on insulator thickness necessary for continued device scaling. Their approach is particularly relevant in the context of advanced MOSFET architectures, including those employing high-κ materials or double-gate configurations, offering a valuable

framework for evaluating the trade-offs in next-generation transistor designs.[2]

Javey et al. (2003) demonstrated a significant advancement in carbon nanotube field-effect transistor (CNTFET) technology by integrating ohmic metal contacts with high-κ HfO_2 gate dielectrics and electrostatically doped source/drain (S/D) segments. This innovative DopedSD - FET structure addresses key limitations of conventional metal S/D Schottky barrier FETs, such as high OFF-state leakage and ambipolar conduction, especially under aggressive vertical scaling. By adopting a MOSFET-like architecture, these CNTFETs exhibit enhanced ON-currents, near-ideal subthreshold swings (~70–80 mV/dec), and suppressed leakage even at high biases and for large-diameter tubes. The work highlights the importance of optimized contact engineering and dielectric integration for achieving scalable, high-performance CNTFETs and establishes a promising path toward next-generation nanoelectronic devices.[3]

Saint-Martin et al. (2004) conducted a comprehensive Monte Carlo simulation-based study comparing different multiple-gate SOI MOSFET architectures—namely single-gate (SG), double-gate (DG), triple-gate (TG), and quadruple-gate (QG)—with gate lengths down to 25 nm. Their work highlights the significant advantages of multiple-gate structures over conventional single-gate designs in mitigating short-channel effects (SCE) and improving electrostatic control. The simulations show that although QG and TG architectures offer the best subthreshold performance and highest ON currents, planar DG MOSFETs strike an optimal balance between performance, integration complexity, and delay metrics. The study emphasizes that effective channel control can be achieved with thinner body devices and that the DG structure, in particular, presents a favourable compromise for future nanoscale CMOS technologies, especially when considering trade-offs between delay, drive current, and off-state leakage.[4]

Li-passivation in zigzag GaN nanoribbons significantly modifies their electronic properties, enhancing Fermi velocity and reducing effective mass to improve carrier mobility. DFT investigations further show strong gas adsorption and charge transfer, highlighting their potential as high-performance nanosensors[5-6].

This paper says that a scalable and industry-compatible method for assembling high-performance integrated devices based on carbon nanotubes (CNTs) and nanowires (NWs) can be achieved without the use of linker molecules. Lee et al. (2006) present a linker -free, surface-patterning approach where inert self-assembled monolayers (SAMs) direct the precise adsorption and alignment of CNTs and NWs onto bare substrate regions. The technique utilizes conventional photolithography and avoids high-temperature processing, making it compatible with standard semiconductor fabrication processes. Notably, the authors demonstrate large-scale fabrication of SWNT- and V_2O_5 NW-based devices, including top-gate transistors and high-density junction arrays with high uniformity and yield. This method provides a practical pathway for integrating nanoscale materials into CMOS-compatible platforms, thereby advancing the realization of hybrid nanowire–silicon electronics.[7]

This paper states that the Berkeley Short-Channel IGFET Model (BSIM) offers a physically grounded yet computationally efficient solution for accurately modeling MOS transistors in advanced integrated circuit design. Developed to address the limitations of earlier SPICE models, BSIM incorporates both strong- and weak-inversion components of the drain current, ensuring continuity and convergence in simulations. It models critical short -channel effects— such as carrier velocity saturation, drain-induced barrier lowering, and depletion charge sharing—while maintaining compatibility with automated parameter extraction processes. By supporting predictive simulation for transistors with effective channel lengths as small as 1 μm, BSIM has become a foundational tool in VLSI design, providing consistent agreement with measured device behavior and enabling reliable digital and analog circuit analysis.[8]

This paper states that the performance of nanoscale MOSFETs is fundamentally governed by scattering effects, which limit the device's ability to achieve ballistic transport. Lundstrom presents a comprehensive scattering theory to model the influence of carrier backscattering on the drain current, introducing the concept of a transmission coefficient (T) to quantify how much of the injected current reaches the drain. Through physical modeling and nonequilibrium Green's function simulations, the study reveals that scattering near the source end of the channel critically reduces the average carrier velocity, while scattering near the drain has minimal impact on current. The paper further establishes that the mean-free-path relative to a small critical region near the source determines how close a device operates to its ballistic limit. This analytical framework provides a foundational understanding for evaluating and optimizing nanoscale transistor performance beyond conventional drift-diffusion models.[9]

This paper states that a fully quantum self-consistent analysis using the Wigner Monte Carlo approach is essential for accurately modeling the behavior of ultimate double-gate (DG) MOSFETs at nanoscale dimensions. Querlioz et al. present a novel simulation framework that incorporates realistic scattering mechanisms and quantum transport effects, offering a more comprehensive alternative to semi-classical and ballistic models. Their results highlight the significant impact of source-to-drain tunneling and quantum reflections on device performance, especially for ultra-short channels and aggressive oxide scaling. Notably, the study finds that despite oxide thinning reducing leakage current, it does not translate into improved delay performance due to increased gate capacitance and limited drive current enhancement. This work underlines the limitations of conventional scaling strategies and emphasizes the need for advanced modeling tools and novel device engineering to meet future technology node requirements.[10]

In the paper titled "High-Frequency Performance Projections for Ballistic Carbon-Nanotube Transistors" by S. Hasan, S. Salahuddin, M. Vaidyanathan, and M. A. Alam, the authors present a comprehensive theoretical and numerical investigation into the high-frequency capabilities of carbon-nanotube field-effect transistors (CNTFETs) operating in the ballistic transport regime. Motivated by early experimental demonstrations of CNTFETs' radio - frequency behavior and the need for predictive modeling, the study employs a quasi -static approach coupled with a ballistic nanotransistor framework to derive a compact equivalent circuit model. This model accurately characterizes the intrinsic device behavior, capturing the unity-current-gain frequency (fT) as a function of gate voltage, and revealing its dependence on key parameters such as gate capacitance and channel length. Analytical results predict that fT can approach a fundamental limit of $vF/2\pi L$ (approximately 130 GHz per micron of channel length), while numerical simulations on MOSFET - like CNTFETs confirm these projections and underscore the importance of device geometry and electrostatics. The work not only identifies theoretical performance limits but also provides a valuable foundation for future design and optimization of high-speed nanoscale transistors.[11]

In the paper titled “Role of Phonon Scattering in Carbon Nanotube Field-Effect Transistors” by Jing Guo and Mark Lundstrom, the authors investigate the impact of phonon scattering mechanisms—both elastic and inelastic—on the performance of short-channel carbon nanotube field-effect transistors (CNTFETs), using a self-consistent Monte Carlo solution of the Boltzmann transport equation. Despite the expectation that short-channel CNTFETs under high bias would suffer performance degradation due to optical phonon (OP) scattering, the study reveals that near-ballistic current levels can still be achieved. This counterintuitive result is attributed to the large energy of optical phonons, which limits backscattering due to Pauli exclusion near the source and significantly reduces the probability of carriers returning after emission. The findings further highlight the unique one-dimensional transport characteristics of CNTFETs, where elastic scattering has a much more pronounced effect than in conventional MOSFETs, particularly if the elastic mean free path is short. These insights are crucial for understanding and optimizing CNT-based nanoelectronic devices under realistic operating conditions.[12]

DFT-based studies demonstrate that Indium Nitride nanoribbons can effectively detect gases like CO, CO_2, NO, and NO_2 due to notable charge transfer and band structure modulation. Similarly, Scandium Nitride monolayers show strong adsorption sensitivity toward toxic gases such as NH_3, AsH_3, BF_3, and BCl_3. Zigzag silicon carbide nanoribbons exhibit enhanced gas sensing performance through improved electronic response to hazardous gas molecules, making them promising for advanced sensor applications[13-15].

In the paper titled “Analysis of CNTFET Physical Compact Model” by C. Maneux et al., the authors present a comprehensive and physics-based compact model for conventional carbon nanotube field-effect transistors (C-CNTFETs), structured similarly to n-type MOSFETs, with the aim of enabling accurate DC simulation for circuit-level applications. A significant contribution of the work lies in the integration of a physical calculation of the conduction subband energy minima, which directly incorporates the influence of carbon nanotube (CNT) helicity and radius—two key parameters that affect the band structure and, hence, the device's electrical behavior. The model is grounded in ballistic one-dimensional transport theory and extends existing frameworks by implementing an analytical formulation of the channel charge and potential that includes quantum capacitance and electrostatics self-consistently. Simulations reveal the substantial impact of CNT diameter and chirality on the drain current characteristics, underscoring the necessity of including such structural considerations in predictive modeling. This model, implemented in Verilog-A and demonstrated using ADS, provides a valuable tool for

the design and evaluation of future CNT-based nanoelectronic circuits.[16]

Density Functional Theory (DFT) investigations reveal that Cu and Fe doping in boron nitride nanoribbons (BNNRs) significantly enhances their electrical conductivity, making them suitable candidates for nanoscale interconnects in advanced integrated circuits. Ab-initio studies on aluminum nitride nanoribbons (AlNNRs) demonstrate their potential in implementing reconfigurable logic gates due to tunable electronic properties under external stimuli. Additionally, the design of a FinFET-based operational amplifier (Op-Amp) using 22 nm high-k dielectric technology shows promising results in reducing leakage currents and enhancing performance, offering a robust solution for low-power, high-efficiency analog circuit applications[17-19].

In the seminal paper "Ballistic Carbon Nanotube Field-Effect Transistors" by Ali Javey, Jing Guo, Qian Wang, Mark Lundstrom, and Hongjie Dai, the authors demonstrate the realization of high-performance, nearly ballistic carbon nanotube field-effect transistors (CNTFETs) by effectively eliminating Schottky barriers at the metal–nanotube contacts through the use of palladium (Pd) electrodes. These Pd contacts, owing to their high work function and strong adhesion to carbon nanotubes, enable ohmic-like behaviour and facilitate carrier injection into the valence band of semiconducting single-walled carbon nanotubes. The resulting devices exhibit room-temperature conductance approaching the ballistic transport limit ($4e^2/h$), high current delivery capability (up to 25 µA per tube), and Fabry–Perot interference patterns at low temperatures—hallmarks of coherent quantum transport. Through experimental comparisons with hydrogen-modified Pd contacts and various channel lengths, the study reveals that short - channel CNTFETs operate near the ballistic limit, while longer channels show increased resistance due to additional scattering. This work establishes a robust framework for CNTFET operation in the ballistic regime, offering significant implications for the future of nanoelectronic devices and transistor scaling strategies.[20]

In the paper titled "Extraordinary Mobility in Semiconducting Carbon Nanotubes" by T. Dürkop, S. A. Getty, Enrique Cobas, and M. S. Fuhrer, the authors present a detailed experimental study on long-channel semiconducting carbon nanotube field-effect transistors (NT-FETs) that demonstrates record-high carrier mobilities, exceeding those of all known semiconductors at room temperature. By fabricating NT -FETs with channel lengths greater than 300 micrometers and Ohmic contacts, the researchers ensure that carrier transport is diffusive and that the device resistance is dominated by the intrinsic nanotube channel rather than contact effects. Their measurements reveal a field-effect mobility as high as 79,000 cm^2/Vs and an estimated intrinsic mobility exceeding 100,000 cm^2/Vs—values significantly higher than those of conventional semiconductors such as silicon or InSb. The paper further confirms the MOSFET-like operation of these devices and attributes the high mobility to minimal phonon scattering and the potential dominance of charged impurity scattering at low gate voltages. These findings highlight the immense promise of semiconducting carbon nanotubes for high-speed and high-sensitivity electronic applications.[21]

In the paper titled "Sorting Carbon Nanotubes by Electronic Structure Using Density Differentiation," Michael S. Arnold, Alexander A. Green, James F. Hulvat, Samuel I. Stupp, and Mark C. Hersam present a scalable and highly effective technique to separate single-walled carbon nanotubes (SWNTs) based on their electronic properties, diameter, and bandgap using density-gradient ultracentrifugation. The study addresses the critical challenge of structural heterogeneity in as-synthesized SWNTs, which impedes their application in nanoelectronics, optics, and sensing. By employing structure-discriminating surfactants—particularly bile salts—the authors exploit subtle differences in buoyant density among nanotube species, enabling the isolation of nearly monodisperse populations of semiconducting or metallic SWNTs. This method achieves remarkable resolution, with over 97% of isolated nanotubes within a 0.02-nm diameter range, and allows for iterative enrichment of specific chiralities such as (6,5) and (7,5). The resulting sorted nanotubes were used to fabricate high-performance thin-film electronic devices, demonstrating clear distinctions in electrical behavior and confirming the effectiveness of the separation. This breakthrough provides a practical pathway for the integration of electronically homogeneous nanotube materials into future technologies.[22]

In the paper titled "An RF Circuit Model for Carbon Nanotubes" by P.J. Burke, the author develops a detailed radio-frequency (RF) circuit model for single-walled carbon nanotubes (SWNTs), portraying them as one-dimensional nano-transmission lines. This model integrates fundamental quantum mechanical effects, including kinetic inductance and both quantum and electrostatic capacitance, to describe the frequency-dependent impedance of carbon nanotubes

across DC to THz regimes. By modeling SWNTs in this way, the paper establishes an electrical engineering framework for analyzing one-dimensional plasmons—the collective charge oscillations characteristic of Luttinger liquids. The study distinguishes between high- and low-damping regimes, explores spin-charge separation due to the nanotube's four conduction channels, and provides predictions for dynamic impedance behavior under various conditions. This work not only bridges concepts from condensed matter physics and RF engineering but also offers foundational tools for the design and analysis of future nanotube-based nanoelectronic and high-frequency systems.[23]

Conclusion

The paper concludes with the validation of a physics-based compact model for CNTFETs, highlighting its accuracy in replicating device behavior and suitability for circuit simulations. The model captures essential quantum effects and provides insight into the impact of CNT structural variations on threshold voltage and delay, making it a valuable tool for designing robust nanoelectronic circuits.

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